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OPEN PROCEDURE WITH APPLICATION OF THE CRITERION OF THE MOST ECONOMICALLY ADVANTAGEOUS OFFER IDENTIFIED ON THE BASIS OF THE BEST QUALITY/PRICE RATIO, PURSUANT TO ARTICLES 71 AND 108 OF LEGISLATIVE DECREE NO. 36/2023 SMI HAVING AS ITS OBJECT THE SUPPLY OF MICROWAVE MEASUREMENT ELECTRONICS FOR THE CHARACTERIZATION OF SUPERCONDUCTING QUBITS FOR THE NQSTI PROJECT IN THE UNIVERSITY COMPLEX OF MONTE SANT'ANGELO, NAPLES

TECHNICAL DOCUMENT RELATING TO THE TENDER FOR THE AWARDING OF A CONTRACT HAVING AS ITS OBJECT THE SUPPLY OF MICROWAVE MEASUREMENT ELECTRONICS FOR THE CHARACTERIZATION OF SUPERCONDUCTING QUBITS FOR THE NQSTI PROJECT

Premise

The intervention in question concerns the purchase of high-tech scientific equipment that will become part of the equipment of the quantum computing and characterization of quantum superconducting devices laboratory of the "Ettore Pancini" Physics Department of the University of Naples Federico II, and will be used for the measurement and control at room temperature of superconducting quantum bits.

This document, attached to the purchase request by the referents for the definition of the technical characteristics is intended to define the technical-functional characteristics suitable to satisfy the needs of the Department.

The equipment and materials supplied must be free of defects, new and original in all their parts and/or components, of the latest generation, complete with all the accessories necessary for the correct functioning of the equipment, as detailed below for each batch.

Used instruments, even in "refurbished" or ex-demo conditions, cannot be offered in the competition.

The elements described represent the minimum required configuration of the Object that the Offeror must comply with in his offer. The listed characteristics must be present simultaneously for the required configuration. Failure to comply with one or more parameters will lead to the exclusion of the offer from the tender.

The required characteristics must be demonstrated in a technical report, produced by the economic operator, which must also contain a detailed description of the equipment offered.

Lot No. 1

Lot No. 1 concerns the purchase of acompact system of room-temperature electronic instruments for the implementation of quantum algorithms on superconducting quantum processor units (QPUs) composed of at least twenty (20) quantum bits.

It must include an integrated instrument solution capable of generating and measuring pulses in the microwave range for the implementation of quantum algorithms and diagnostic protocols on at least twenty superconducting qubits, with the following general characteristics:

- Quantum Non-Destructive (QND) readout of the state of qubits, i.e. capable of generating and measuring low-power microwave signals in the range from 100 MHz to > 9 GHz;
- control of superconducting qubits from 100 MHz to > 9 GHz, capable of generating low-power signals in order to avoid transitions to non-computational higher energy levels in superconducting qubits;
- frequency tuning, i.e., low-noise current/voltage arbitrary waveform generators, used to tune the electrodynamic parameters of the QPU by external flux. Low noise is a key requirement for reducing phase shift and decoherence in the QPU. Low-noise, ultra-stable DC current offset sources are required to generate the offset for the flux pulses. These signals need to be bias-coupled with fast AWG (Arbitrary Waveform Generator) channels in the > 250 MHz base band regime.

The following services must be an integral part of the requested supply:

- Transport, delivery, installation, commissioning of the instrument and verification of conformity.
- Warranty service, support and a preventative maintenance plan included in the standard 36-month warranty period.
- Training of personnel in the use of the acquired equipment for a minimum duration of two days.

Technical and functional characteristics of lot no. 1: Microwave measurement electronics for the characterization of superconducting qubits

Specifications:

Specifications on key components: readout and control tools, tuning, and data acquisition/processing specifications.

Specifications of the reading modules (minimum 5 RF pulse signal inputs/outputs)

- Operating frequency range 100 MHz to > 9 GHz, such that it is compatible with cryogenic amplifier electronics and cryogenic input and output readout signal lines in a dilution cryostat. Frequency resolution shall be ≤ 1Hz.
- Up- and down-conversion solutions for direct RF pulse generation must be integrated into the system (local oscillators and IQ mixers and/or digital mixers), without the need for additional hardware.
- 1GS/s DAC-ADC speed, for high-performance pulsed readout schemes in superconducting qubits.

- In case of an analog solution for analog up- and down-conversion, the possibility of self-calibration for the suppression of local oscillator losses and IQ mixer corrections must be ensured.
- In the case of digital mixing solutions, automatic signal optimization without the need for calibration must be ensured, combining Direct Digital Synthesis (DDS) and single mixing for high-level performance across the entire frequency range.
- Minimum read pulse width of 4 ns with rise/fall timemaximum of 1.4 ns (10% - 90%).
- The ability to change arbitrary pulse shapes and their parameters in real time with a maximum update rate of 4 ns must be ensured. Pulse widths, offset, modulation phase and gain must be programmable via FPGA.
- The input channels must allow on-board processing of the measurement with typical averaging and integration functions, and must allow thresholding processes.
- It shall be possible to assign arbitrary pulse shapes and integration functions in order to minimize crosstalk and improve QPU readout fidelity.
- For output signals, a SFDR (Spurious Free Dynamic Range) > 40 dB is requiredin the range from 100 MHz to > 10 GHz
- For output signals, the phase noise must satisfy the following conditions:
    - < -110 dBc /Hz at 5 GHz and 10 kHz offset;
    - < -140 dBc /Hz at 5 GHz and 10 MHz offset;
- The readout channels shall have the capability of multiplexed readout of at least 6 frequency tones in a bandwidth > 750 MHz. To support scalability, instrumentation capable of multiplexed readout of at least 8 tones shall be preferred. Each frequency channel (resonator) in the multiplexed input shall be processed individually by the FPGA for acquisition of measurement results from each qubit. Each frequency channel must be adjusted individually and independently within the same module, therefore for the same input/output pair for reading.
- It shall be possible to combine channels to increase the bandwidth > 1.6 GHz.
- The input channels shall allow signals down to -26 dBm to operate in the single-photon regime, and provide a variable-gain input stage with >25 dB of tuning.
- The probe radiation tones of the readout resonators shall be generated by the FPGA, allowing full control of amplitude, offset, modulation frequency and phase.
- SMA input-output connectors.
- Readout memory for > 100,000 I/Q values per qubit.

The following specifications are also required:

- Fully integrated solutions where the IQ channels are internally integrated with up- and down-conversion stages for the RF output channels.
- Solutions where real-time operations are programmed in a completely deterministic way with the possibility of back-to-back playback of pulses without intermediate delays.

Control Module Specifications (minimum 20 RF pulse signal outputs to control 20 qubits simultaneously)

- Operating frequency range from 100 MHz to >9GHz, compatible with typical superconducting qubit frequencies and different circuit designs. The frequency resolution will have to be ≤ 1Hz.
- Control channels will need to allow output in the low-power regime from -40 dBm to 5 dBm to avoid leakage to higher-order non-computational levels in superconducting qubits.
- Digital mixing solutions based on the combination of Direct Digital Synthesis (DDS) and single mixing, to ensure automatic signal optimization without the need for calibration.

- 5GS/s DAC rate, for high-performance fast control pulsed schemes in superconducting qubits.
- Minimum width of the control/guidance pulse4 ns withMaximum rise/fall time of 1.4 ns (10% - 90%)
- Control channels shall allow multiplexed output of at least 8frequency tonesin a bandwidth of >800 MHz, while each drive frequency channel can be individually controlled with real-time pulse parameters such as amplitude, offset, modulation frequency and phase.
- Ability to modify arbitrary pulse shapes and their parameters in real time for the implementation and correction of single- and multi-qubit gates, including virtual-Z gates, with up to 4 ns update rate. Pulse widths, offset, modulation phase, and gain shall be programmable via FPGA.
- Pulses shall be selectable from local memory, rather than by loading from a host PC. Local wave memory shall allow the definition of pulses with arbitrary shapes in a 1 ns time grid.
- Spurious Free Dynamic Range (SFDR) > 40 dB in the intervalfrom 2GHz to >9GHz.
- For output control signals, the phase noise must satisfy the following conditions:
    - < -110 dBc /Hz at 5 GHz and 10 kHz offset;
    - < -140 dBc /Hz at 5 GHz and 10 MHz offset;
- Signal to Noise Ratio (SNR) at 1.5 GHz > 150 dB.
- SMA input-output connectors.

They are also requiredthe following specifications:

- Solutions where real-time operations are programmed in a completely deterministic way with the possibility of back-to-back playback of pulses without intermediate delays.

Flow Tuning Module Specifications (minimum 20 DC output sources and minimum 20 pulsed voltage outputs)

- Output range for current sources with flux offset >±50 mA, with 16-bit DAC resolution.
- Output voltage for pulsed flow signals >4.5Vpp in the frequency range from DC to > 250 MHz.
- Ability to modify arbitrary flow pulse shapes and their parameters in real time with a maximum update rate of 4 ns. Pulse widths, offset, modulation phase and gain shall be programmable via FPGA.
- The flow pulses shall be selectable from a local wave memory to avoid loading from the host PC. The local wave memory shall allow the definition of flow pulses with arbitrary shapes in a 1 ns time grid.
- Minimum amplitude of voltage flux-pulse of4ns with maximum rise/fall time of 1.4 ns (10%-90%).
- Step response with < 0.5% overshoot. This should be shown explicitly via output graphs.
- The flow offset noise should have the following requirements:
    - measured at +50 mA into 50 Ω with range ±50 mA:
        - <2.5 nA/√Hz at 10 Hz;
        - <0.8 nA/√Hz at 1 kHz;
- ThereVoltage noise density for 1 Hz flux pulses on a 50 W loadoh must be < 1.5μV/Hz1/2.
- Stability of offset voltages of the flow-voltage pulse generatormust be<1.5 ppm/K, referred to full scale.
- A monitoring system for the generated offset currents must be available through a dedicated voltage monitoring output.
- The voltage sourceof exitof driftfor flow offsetmust have the following requirements:
    - measured at +50 mA on 50ohwith ± 50 mA range: < 2.5 ppm/°C full scale.

- For the flow offsetsystems are needed to avoid ground loops and to prevent interference (e.g. no physical connection between the ground network and the output channels, isolation systems, etc...). For example,the power supply may include gyrator filters to avoid ground loop problems.
- Since sources with flow offset do not require rapid synchronization with the host PC,USB connection is a possible alternative to Ethernet/LAN connection.
- Backup batteries must be supplied with DC sources.with flow offset.

They are also requiredthe following specifications:

- Higher voltage outputs for flux tuning, to omit bias-tee coupling between DC sources and AWG outputs.
- Specification of AWG flux pulse modules compatible with typical control pulse generators, in order to provide direct control as the number of qubits increases.
- Dedicated isolation (galvanic or similar) applied to the mains supply of the flow offset and/or pulsed flow outputs to avoid ground loops and interference.
- DC sources powered directly by batteries, which are automatically charged via a constant connection to the grid. It must be ensured that the batteries are recharged in the same unit, without necessarily disconnecting them from the system, to avoid interruption of the experiment.
- Flow pulse generation solutions where real-time operations are scheduled in a fully deterministic manner with the possibility of back-to-back pulse playback without intermediate delays.

Data acquisition/processing specifications

- Internal/External Trigger Tools:
    - The system shall incorporate a 10 MHz reference clock where all local oscillators, FPGAs and other system clocks are phase-locked.
    - Ability to insert external clock sources as 10 MHz master clock or output the internal clock via SMA, USB or equivalent input-output connectors for synchronization of external devices.
    - Digital outputs, as well as analog outputs for triggering external devices, shall accompany the control lines. The timing of the generated pulses shall be synchronized in a standard manner with other laboratory equipment from other manufacturers. The trigger input shall be incorporated to receive marker/trigger signals from external devices.
- The FPGA-supported parameterization of the generated pulses will need to operate fully deterministically, with real-time pulse generation and parameter updates for the control, readout, and pump pulses, as described above. FPGAs will need to incorporate sufficient memory to store local waves and instructions for typical experiments for controlling and reading qubits.

Programming for interface with instruments

- All driver/API and interface layers must support the Python programming language.
- Along with low-level access, high-level programming should be possible for intuitive programming of pulse-level and gate-level definitions of pulses and qubit operations, including writing hardware diagnostic codes of quantum circuits.

- Automated calibration routines for typical quantum computing experiments, e.g. internal self-calibration tools for local oscillator leakage suppression and IQ mixer corrections.
- Software tools are required for convenient coding, easy debugging, oscilloscope mode and visualization tools.

They are also requiredthe following specifications:

- Drivers and parameters will need to be controlled using open source drivers compatible with QCoDes and Quantify packages and drivers.
- Ability to program FPGA using VHDL(VHSIC - Very High Speed Integrated Circuit - Hardware Description Language)or alternative methods for low-level access to FPGAswithout VHDL.
- Ability to create wrappers around the Python API (Application Programming Interface),or around the low-level programming interface.
- Open source software levels, for both high-level and low-level programming.

Programming for data acquisition, diagnostic procedures, calibration and analysis

- Free one week training program: A one-week training program shall be provided to instruct users and lab members for rapid setup and start of measurements in the first week of delivery. Tutorials, typical experimental notebooks, and example code scripts shall be provided for reference.
- Aside from the low-level programming, API layers, and diagnostic toolset mentioned above, the system must be equipped with a high-level software package that allows the full functionality of the hardware to be exploited. It must be possible to write any program arbitrarily, to create arbitrary pulse sequences and readout patterns within the constraints of the hardware. This high-level software must be open-sourced to create proprietary algorithms in addition to the functionality mentioned above.
- The high-level software must support QCoDeS drivers to integrate it with other existing experimental hardware systems and software frameworks..

They are also required the following specifications:

- The software and/or programming scripts must be open-source and customizable by the user if necessary.
- The hardware will need to be compatible with Python scripts that leverage the Quantify library for code reuse currently in use by the research group.

It must be guaranteed:

- Ethernet/LAN, and/or data connectionequivalent, between the instruments and a host PC, with data speeds of at least 1 GBit/s.
- A modular system where input and output channels can be added on demand. It is preferable to have a system where the same hardware backplane, timing, feedback, software levels and other features are maintained as the system grows in size.
- Synchronization of all channels for read/control/tunable signals with timing less than 1 ns,with a jitter of a few ps,without the need for additional hardware equipment.
- The measurement results must be distributed among the modules with low-latency feedback for the implementation of fast and reliable single- and multi-qubit gates, quantum error correction schemesand for the distribution of channels of at least 20 qubitswith all-

to-all connectionin the same time window.Independent control of each sequencer and channel is required. Feedback operations must be performed between all control and readout channels internally, without the need for an external central unit, repeater or synchronization module.

- The system must be compatible witha well-documented and professionally maintained Python-based software stack to control the QPU experiments. Hardware control software is required to allow programming of all the features and input and output channels as described in the following sections. The user will have full access to the source codes and will have permissions to modify and develop the codes in the future.

The ability to synchronize all channels in the instruments/modules within the hardware (via backplane, internal connections) is required, without the need for additional wiring between separate hardware units. The system shall be able to scale up to 100+ qubits with the same synchronization framework.

System voltage: power supply of 215-230 V/50Hz. Maximum power absorbed at full load of approximately 5 kW.

Racks: The system must be equipped with a tool rack, where all the tracked products will be placed. The possibility of having an additional solution to ensure flexibility for the needs of the research group is appreciated.

Lifetime remote technical support.

- The economic operator shall describe the technical support channels during the warranty period. The technical support channels shall provide answers no later than 48 hours after the questions are sent via email/phone/other, during the warranty period.
- Describe product maintenance or product replacement during the warranty period.
- The economic operator will have to provide firmware updates that can be executed even without direct support from the same.

Free system support and maintenance for the first 3 years.

Lead time: 6 months from order confirmation.